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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,009	02/02/2001	Michael A. Vyvoda	MA-027	7430

33971 7590 05/12/2004

MATRIX SEMICONDUCTOR, INC.
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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/776,009	VYVODA ET AL.	
	Examin r	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cov r sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14,30-34,36-48 and 50-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14,30-34,36-48 and 50-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Amendment filed February 17, 2004 has been entered. Claims 1, 30 and 44 have been amended. Claims 57-62 have been added. Claims 1-5, 7-14, 30-34, 36-48 and 50-62 are pending.

Claim Objections

2. Claims 8, 10, 12-14, 39-43 are objected to because of the following informalities: these claims recite the term "semiconductor", the correct term should be "polysilicon semiconductor".

Appropriate correction is required.

3. Claims 58, 60 and 62 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

The limitation of "doped polysilicon" have been recited by claims 57, 59 and 61.

Claim Rejections - 35 USC § 102/103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims **1**-5, 7, 12, 14, **30**-34, 36, 41, 43-48, 50, 54 and 56-62 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bergemont et al. (U.S. Patent No. 6,290,010).

With respect to claims **1, 30** and **44**, insofar the device is concerned and as best understood by the examiner, Bergemont teaches a wafer having a surface as claimed including:

a plurality of regions of dielectric (or means for attracting water, or hydrophilic material) (406) and polysilicon semiconductor (or means for repelling water, or hydrophobic material) (412) exposed at the surface of the wafer (400) the polysilicon semiconductor regions (412) formed over the wafer (400), wherein

the polysilicon semiconductor regions (412) have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer (400) and

each of the polysilicon semiconductor regions (412) have a shortest surface dimension that is less than or equal to a first width,

the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom,

and wherein the surface is planarized. (See Figs. 14).

Product by process limitation:

The expressions "after chemical mechanical planarization" and "allowing removal of residual particles therefrom" are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324,

326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Since the surface of the polysilicon (412) and dielectric region (406) are planarized, the limitation of the claim is met.

With respect to the functional limitation: "the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom", since the polysilicon semiconductor regions (412) have a total surface area that is less than or equal to a first fraction and the first width, thus, the wafer having a surface of Bergemont should inherently function as claimed.

With respect to claims 2, 3, 31, 32, 45 and 46, although not explicitly disclose, however, as shown in Fig. 7, the polysilicon semiconductor region (412) of Bergemont is definitely less than 50 or 60% total surface area of the wafer.

With respect to claims 4, 5, 33, 34, 47 and 48, the polysilicon semiconductor region (412) of Bergemont is formed in an the via of 0.25 μm (col. 4, lines 60-67), thus, definitely less than 2.5 millimeters and 500 μm.

With respect to claims 7, 36 and 50, the dielectric regions or the means for attracting water or the hydrophilic material (406) of Bergemont comprises silicon dioxide.

With respect to claims 12, 41 and 54, the regions of polysilicon semiconductor or the means for repelling water or the hydrophobic material (412) of Bergemont are rectangular.

With respect to claims 14, 43 and 56, the region of polysilicon semiconductor or the hydrophobic material (412) of Bergemont are interspersed within a sea of dielectric (406). (See Fig. 7).

With respect to claims 57-62, the polysilicon semiconductor regions or the means for repelling water or polysilicon hydrophobic material (412) of Bergemont comprises doped polysilicon.

Product by process limitation:

The expression "the doped polysilicon is doped by depositing a dopant along with polysilicon" (claims 58, 60 and 62) is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the polysilicon semiconductor regions or the means for repelling water or polysilicon hydrophobic material (412) of Bergemont comprises doped polysilicon. Thus, the limitation of the claims are met.

5. Claims **1**-5, 7-12, **30**-34, 36-41, **44**-48, 50-54 and 57-62 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Sardo et al. (U.S. Patent No. 5,032,881).

With respect to claims **1, 30** and **44**, insofar the device is concerned and as best understood by the examiner, Liu teaches a wafer having a surface as claimed including:

a plurality of regions of dielectric (or means for attracting water, or hydrophilic material) (270) and polysilicon semiconductor (or means for repelling water, or hydrophobic material) (258) exposed at the surface of the wafer (252) the polysilicon semiconductor regions (258) formed over the wafer (252),

wherein the polysilicon semiconductor (258) regions have a total surface area that is less than or equal to a first fraction of a total surface area of the wafer (252) and

each of the polysilicon semiconductor regions (258) have a shortest surface dimension that is less than or equal to a first width,

the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom,

wherein the surface is planarized. (See Figs. 4-5).

Product by process limitation:

The expressions "after chemical mechanical planarization" and "allowing removal of residual particles therefrom" are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324,

326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Since the surface of the polysilicon (258) and dielectric region (270) are planarized, the limitation of the claim is met.

With respect to the functional limitation: "the first fraction and the first width ensuring that the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom", since the polysilicon semiconductor regions (258) have a total surface area that is less than or equal to a first fraction and the first width, thus, the wafer having a surface of Sardo is more probable than not function as claimed.

With respect to claims 2, 3, 31, 32 , 45 and 46, the polysilicon semiconductor region (258) of Sardo having a shortest dimension of 0.8 μm and the width of the dielectric region (270) is also 0.8 μm, thus, the limitation of the claims, less than or equal to 50 %, are met.

With respect to claims 4, 5, 33, 34, 47 and 48, the polysilicon region (258) of Sardo is 0.8 μm, less than 500 μm or 2.5 millimeters,

With respect to claims 7, 36 and 51, the dielectric region (270) of Sardo comprises silicon dioxide.

With respect to claims 8, 39 and 50, the regions of dielectric (270) and polysilicon (258) of Sardo are alternate along the surface of the wafer. (See Fig. 5).

With respect to claims 9, 10, 37, 40 and 52, the regions of dielectric (or the means for attracting water) (270) and the polysilicon semiconductor (or the means for repelling water) (258) of Sardo are elongated strips. (See Fig. 5).

With respect to claims 11, 12, 38, 41, 53 and 54, the dielectric region (270) and the polysilicon region (258) of Sardo are elongated strips, thus, rectangular.

With respect to claim 57-62, the polysilicon semiconductor regions (258) of Sardo comprise doped polysilicon.

Product by process limitation:

The expression "the doped polysilicon is doped by depositing a dopant along with polysilicon" (claims 58, 60 and 62) is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the polysilicon semiconductor regions or the means for repelling water or polysilicon

hydrophobic material (258) of Sardo comprises doped polysilicon. Thus, the limitation of the claims are met.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 13, 42 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont '010 as applied to claims 1, 30 and 44 above, and further in view of Inoue (U.S. Patent No. 4,656,054) of record.

Bergemont teaches the polysilicon hydrophobic semiconductor regions (412) having rectangular shape.

Thus, Bergemont is shown to teach all the features of the claim with the exception of form the polysilicon semiconductor regions (412) having an alternate shape such as of hexagon.

However, Inoue teaches semiconductor regions can be formed in to various shapes using a mask having various shapes including hexagon. (See Fig. 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the polysilicon semiconductor region of Crafts having hexagonal shapes as taught by Inoue because more polysilicon semiconductor island having hexagonal shape can be made in a given area (Fig. 8) than the other shapes. (See Figs. 5 and 6).

Response to Arguments

7. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A.M
May 6, 2004

LONG PHAM
PRIMARY EXAMINER